REMARKS

This is intended as a full and complete response to the Final Office Action dated April 13, 2005, having a shortened statutory period for response set to expire on July 13, 2005. Applicant submits this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

In the specification, paragraph [0067] has been amended to correct minor editorial problems.

Claims 12-14 have been cancelled without prejudice. Claims 1-11 and 15-20 remain pending following entry of this response. Claims 1 and 6 have been amended. Applicant submits that the amendments do not introduce new matter.

Claim Objections

Claims 6, 7 and 12-14 are objected to because of informalities. Claim 6 has been amended as suggested in the Office Action. Claims 12-14 have been cancelled. Accordingly, Applicant requests withdrawal of this objection.

Claim Rejections - 35 USC § 102

Claims 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by *Sakagami* (JP 62-40816). Applicant has cancelled claims 12-14 and requests withdrawal of this rejection.

Claim Rejections - 35 USC § 103

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sakagami* (JP 62-40816) in view of *Weste et al.* (Principles of CMOS VLSI Design: A Systems Perspective, 1993, Addison Wesley, 2nd Edition, page 91, hereinafter "*Weste*"). Applicant respectfully traverses this rejection as follows.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill

in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP § 2143.

Regarding the first criterion for establishing a *prima facie* case of obviousness, Applicant submits there is no suggestion or motivation to combine the references as suggested in the Office Action. The Examiner relies on Figure 14 of *Sakagami* as teaching all elements of the claimed flip-flop, except that the claimed second signal path includes a delay element in the form of a transmission gate. The Examiner, however, relies on *Weste* as teaching a transmission gate and states "it would have been obvious to one having skill in the art at the time the invention was made to implement each of the tristate inverters in Figure 14 of the *Sakagami* reference by cascading a transmission gate with an inverter" as taught in *Weste*. However, even assuming that *Sakagami* could be modified in the manner suggested by the Examiner does not make the modification obvious absence a suggestion of the desirability of the modification. See MPEP § 2143.01.

As described in paragraph [0067] of the present application, a delay element, such as the claimed transmission gate, may help prevent a condition where an inverted data signal is transferred from the second node to the third node upon the falling edge of the clock signal, which may bring about an unstable state in the second feedback loop. This condition may occur because the claimed structure generates inverted and non-inverted data signals from a single data input.

Sakagami, on the other hand, utilizes two separate data inputs for non-inverted and inverted data signals. As a result, in *Sakagami*, there is no possibility the above-described situation will occur, as the signals at the third and fourth nodes of the second holding element are always inverted with respect to each other (i.e., complementary). Consequently, a person skilled in the art would not be motivated to include an unnecessary delay element in the second signal path, as claimed.

Regarding the third criterion for establishing a *prima facie* case of obviousness, Applicant submits that, even if combined as suggested in the Office Action, *Sakagami* and *Weste* would not teach or suggest all the claim limitations. For example, even if the

transmission gate of *Weste* were combined with *Sakagami*, there is no teaching in either reference that the transmission gate would be *permanently switched on when the device is in a normal operating mode*, as claimed. As shown in Figures 7 and 8 of the present application, depending on the embodiment, the transmission gate may be permanently switched on during normal operation by coupling the transmission gate inputs to power and ground (see Figure 7) or to complementary versions of a reset signal (see Figure 8).

Accordingly, Applicant submits claim 1, as well as claims 2-4 depending therefrom, are patentable over *Sakagami* in view of *Weste*, and requests withdrawal of this rejection.

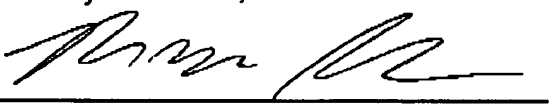
Allowable Subject Matter

Claims 5, 8-11 and 15-20 have been allowed. Claims 6 and 7 would be allowed if amended to overcome the informalities described with reference to the objection above. Claims 6 and 7 have been amended as described above. Accordingly, Applicant submits these claims are now in condition for allowance.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted,



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